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Atty. Docket No. OPP031367US

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF:	:
Kang-Hyun LEE	: GROUP ART UNIT: 2813
APPLICATION NO: 10/728,706	:
FILED: DECEMBER 5, 2003	: EXAMINER: NGUYEN, Tuan H.

FOR: METHOD FOR FABRICATING METAL LINE OF SEMICONDUCTOR DEVICE

I hereby certify that this document is being facsimile transmitted to the USPTO or deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 1-12-06

By: Jennie Heaton
Jennie Heaton

DECLARATION UNDER 37 C.F.R. 1.132

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SIR:

Now comes Kang-Hyun LEE, who declares and states that:

1. I am the sole inventor of the subject matter disclosed and claimed in the above-identified application. My qualifications are attached hereto as Exhibit A.

2. I have read the above-identified application. I have also reviewed U.S. Patent No. 6,383,942 to Narita et al. (hereinafter, "Narita") and U.S. Patent No. 6,750,150 to Chung et al. (hereinafter, "Chung").

3. I understand that the broadest claim of the above-identified application is directed to a method for fabricating a metal line of a semiconductor device, comprising the steps of:

a) forming an insulation layer on a semiconductor substrate on which devices or lower lines are formed;

b) forming a metal layer on the insulation layer;

c) forming a photoresist pattern having an opening of certain width on the metal layer, wherein the photoresist has a thickness of less than 9000 Å and a ratio of the photoresist thickness to the width of the opening is less than about 3.5;

d) forming a buffer layer on the photoresist pattern, including in the opening; and

e) selectively removing the metal layer at a lower side of the opening by dry etching to form a plurality of metal lines such that a dimension between adjacent metal lines is less than the width of said opening.

4. The method defined by steps a)-e) in paragraph 3 above shows unexpected improvements in defect reduction relative to otherwise identical methods in which no buffer layer is formed on the photoresist pattern and:

(i) The photoresist has a thickness greater than 9000 Å and a ratio of the photoresist thickness to the width of the opening is greater than about 3.5; or

(ii) The photoresist has a thickness less than 9000 Å.

5. For example, step c) in paragraph 3 above recites "selectively removing the metal layer at a lower side of the opening by dry etching to form a plurality of metal lines." In processes used to manufacture commercial semiconductor devices, to form a plurality of metal lines successfully, gaps between adjacent metal lines are formed without defects that cause a short circuit between the adjacent metal lines.

6. In processes used to manufacture commercial semiconductor devices in which a critical dimension between adjacent metal lines is 0.26 μm or less, a problem arises when the photoresist has a thickness greater than 9000 Å.

7. In this case, the openings in the photoresist have an aspect ratio (i.e., the ratio of the photoresist thickness to the width of the opening) of greater than about 3.5. In other words, since 9000 Å/2600 Å (0.26 μm) is about 3.5 (using 2 significant digits), a photoresist thickness of > 9000 Å divided by a width of 0.26 μm leads to an aspect ratio of > about 3.5.

8. When the openings in the photoresist have an aspect ratio > about 3.5, the aspect ratio of the gap formed between adjacent metal lines having relatively thick photoresist thereon increases. This increase results in an increased likelihood of the formation of metal "stringers" or other defects at the bottom of the gaps between the resulting metal lines that result in a short circuit between adjacent metal lines.

9. In the case where the photoresist has a thickness greater than 9000 Å and the openings in the photoresist have an aspect ratio > about 3.5, the increased likelihood of metal "stringers" or other short circuit-causing defects is unacceptably high for a commercial manufacturing process.

10. One possible solution to this metal "stringer" problem is to reduce the photoresist thickness to less than 9000 Å. (In a commercial semiconductor manufacturing process, one generally cannot reduce the metal layer thickness without adversely affecting performance of the manufactured semiconductor devices.) However, in many commercial semiconductor manufacturing processes, a thickness of less than 9000 Å for a conventional photoresist may not be sufficient to dry etch the metal layer under the photoresist (see step c) in paragraph 3 above).

11. Typical conditions for dry etching a metal layer in commercial semiconductor manufacturing processes are generally not sufficiently selective with respect to the photoresist to ensure that an adequate amount of photoresist remains over the metal layer to prevent inadvertent etch damage to the top of the metal layer. Thus, when the photoresist thickness is less than 9000 Å in commercial CMOS semiconductor manufacturing processes, there is an increased likelihood of damage to the upper surfaces of the resulting metal lines

that can degrade performance of the resulting semiconductor devices and/or adversely affect subsequent processing (e.g., anti-reflective coatings formed at or on the upper surface of the metal lines may have unacceptable anti-reflective properties).

12. In this case, the increased likelihood of dry etch damage to the upper surface of the metal lines is unacceptably high for a commercial semiconductor manufacturing process.

13. To solve these "metal stringer" and dry etch damage problems, the method recited in paragraph 3 above first forms a photoresist pattern on the metal layer, where the photoresist has a thickness of less than 9000 Å and a ratio of the photoresist thickness to the width of an opening in the photoresist is less than about 3.5, then forms a buffer layer on the photoresist pattern, including in the opening.

14. The method recited in paragraph 3 above reduces the likelihood of "metal stringer" (or other short circuit-causing) defects and any adverse effects from dry etch damage to an upper surface of metal lines to levels or values that are acceptable for commercial semiconductor manufacturing processes.

15. One of ordinary skill in the art of semiconductor manufacturing would not understand or appreciate from reading the Narita and Chung patents that the method recited in paragraph 3 above would provide the observed improvements in defect reduction (i.e., from commercially unacceptable levels to commercially acceptable levels).

16. For example, Narita discloses a dry etching method for use in patterning stacked metal films containing aluminum as the base component and a thin film including at least one of titanium and titanium nitride (Abstract). The method of Narita intends to provide a dry etching method capable of patterning a stacked film such that the thin film is formed vertically, and the metal film is prevented from being side-etched (col. 2, ll. 47-53) and/or a pattern transfer difference is reduced in the stacked film (col. 3, ll. 1–4).

17. Narita teaches that the width of processed wiring usually becomes larger than that of a mask when a mask pattern is formed on the stacked film, and then the stacked film is processed by dry etching (col. 10, ll. 18-21). In such a case, it is likely that an interval (or gap) between wiring portions will be narrowed, and a short circuit will be caused easily

between them (Narita, col. 10, ll. 21-24). This disclosure is consistent with the discussion in paragraphs 8-9 above regarding the "metal stringer" problem.

18. Narita further teaches that this problem is difficult to solve in miniaturized devices using conventional approaches (col. 10, ll. 35-36). For example, the wiring cannot be thinned because its resistance is increased, and accordingly, the photoresist mask pattern cannot be reduced in thickness (Narita, col. 10, ll. 36-41). Consequently, Narita teaches that the mask is narrowed and the photoresist mask aspect ratio is increased, resulting in a phenomenon in which the mask pattern is easy to physically fall when it is washed after development (col. 10, ll. 41-45). This disclosure is consistent with the discussion in paragraph 10 above regarding problems resulting from conventional solutions to the "metal stringer" problem.

19. Narita appears to be silent with regard to forming a buffer layer on a photoresist pattern. Accordingly, Narita cannot suggest the observed improvements in defect reduction provided by the method recited in paragraph 3 as a result of forming a buffer layer on a photoresist pattern.

20. Chung discloses a semiconductor manufacturing method that includes defining a substrate, depositing a polysilicon layer over the substrate, depositing a layer of photoresist over the polysilicon layer, patterning and defining the photoresist layer, depositing a layer of inorganic material over the patterned and defined photoresist layer where the layer of inorganic material is conformal and photo-insensitive, and anisotropically etching the layer of inorganic material and the layer of semiconductor material (Abstract).

21. While it is an object of the invention of Chung to enhance the etching resistance of a patterned photoresist layer (col. 1, ll. 37-39), Chung appears to be silent with regard to any defect reduction effects of forming the layer of inorganic material over the patterned and defined photoresist layer. Accordingly, Chung cannot suggest the observed improvements in defect reduction provided by the method recited in paragraph 3 as a result of forming a buffer layer on a photoresist pattern.

22. As a result, the observed improvements in defect reduction provided by the method recited in paragraph 3 are unexpected in view of the Narita and Chung patents.

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Further, Declarant sayeth not.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the above-identified application or any patent issued thereon or therefrom.

Kang-Hyun LEE

2005. 12. 12.
Date

EXHIBIT A

Work Experience:

. 2001. 5. – Present: DongbuAnam Semiconductor, Inc., responsible for production engineering 2team.

. 1998. 1. ~ 2001. 4.: GSDC(Gigarams semiconductor design company), at Taiwan, responsible for PE engineering.

. 1989. 2. ~ 1997. 12.: Samsung Electronics, Inc., Senior etch process engineer at R & D center.

Education: Received a B.S. degree in Physics from Sogang University in 1989. 2.